In the Claims:

This listing of claims will replace all prior version and listings of claims in the application:

1 - 18. Cancelled.

19. (Previously presented) An integrated electronic device comprising:

a semiconductor body having a substrate;

a pair of insulation structures disposed in the substrate, delimiting an active area of the substrate, and each having a respective portion projecting from said substrate, the projecting portions defining a recess over a portion of the active area and over a portion of at least one of the insulation structures, said recess having a substantially constant width throughout its vertical dimension; and

a memory cell having a body region disposed in the portion of the active area, a gate insulator disposed over the body region, a floating gate disposed in the recess over the gate insulator and over the portion of the at least one insulation structure such that the floating gate does not extend above the projecting portions of the insulating structures, and a control gate disposed over the floating gate.

20. (Previously presented) The device according to claim 19 wherein:

said projecting portions define the recess over respective portions of both of the insulation structures; and

said floating gate is disposed over the respective portions of both the insulating structures.

21. Cancelled.

22. (Previously presented) The device according to claim 19 wherein said floating gate does not extend laterally beyond the projecting portions of the insulating structures.

23. (Previously presented) The device according to claim 19 wherein said floating gate has a surface facing the control gate, the entire surface being planar.

24 – 25. Cancelled.

26. (Previously presented) An integrated circuit, comprising:

a substrate having an active region;

first and second insulators disposed adjacent to the active region and defining a recess over a portion of the active region and over a portion of at least one of the first and second insulators, said recess having first and second sides that are substantially perpendicular to the surface of the active region;

a body region of the memory cell disposed in the portion of the active region;

a first gate insulator disposed over the body region; and

a floating gate of the memory cell disposed in the recess over the gate insulator and over the portion of at least one of the first and second insulators but not extending beyond the recess in a dimension parallel to a surface of the active region.

27. (Original) The integrated circuit of claim 26 wherein the first and second insulators respectively comprise first and second projections that define the recess.

28. (Original) The integrated circuit of claim 26, further comprising:

first and second trenches disposed in the substrate; and

wherein the first and second insulators are respectively disposed in the first and second trenches.

29. (Original) The integrated circuit of claim 26 wherein the first and second insulators define the recess over respective portions of both the first and second insulators.

30. Cancelled.

31. (Previously presented) The integrated circuit of claim 26 wherein the floating gate does not extend above the first and second insulators.

32. Cancelled.

33. (Previously presented) The integrated circuit of claim 26, further comprising:

a second gate insulator disposed on the floating gate; and

a control gate disposed on the second gate insulator and overlapping the floating gate.

34. (Previously presented) An integrated circuit, comprising:

a substrate;

a first isolation region disposed in the substrate and defining a recess that is bounded by the first isolation region on at least two sides, the first isolation region having a first depth beneath the recess and a second depth outward from the recess along at least one of the at least two sides, the first depth being greater than or equal to the second depth; and

a first conductor disposed in, and extending no higher than, the recess.

35. (Original) The integrated circuit of claim 34 wherein the first insulator comprises projections that define the recess.

36. (Original) The integrated circuit of claim 34, further comprising:

a trench disposed in the substrate; and

wherein the first insulator is disposed in the trench.

37. (Original) The integrated circuit of claim 34 wherein the first conductor composes a resistor.

38. (Original) The integrated circuit of claim 34 wherein the first conductor composes a plate of a capacitor.

39. (Previously presented) An integrated circuit, comprising:

a substrate;

a first isolation region disposed in the substrate and defining a recess that is bounded by the first isolation region on at least two sides, the first isolation region having a first depth beneath the recess and a second depth outward from the recess along at least one of the at least two sides, the first depth being greater than or equal to the second depth;

a first conductor disposed in the recess;

a second insulator disposed on the first conductor; and

a second conductor disposed on the second insulator and overlapping the first conductor.

40 - 48. Cancelled.

49. (Previously presented) An integrated circuit, comprising:

a substrate having an active region;

first and second insulators disposed adjacent to the active region and defining a recess over a portion of the active region and over a portion of at least one of the first and second insulators;

a body region of a memory cell disposed in the portion of the active region;

a first gate insulator disposed over the body region; and

a floating gate of the memory cell disposed in the recess over the gate insulator and over the portion of one of the insulators, the floating gate having a substantially constant width throughout its vertical dimension.